first and second impurity diffusion layers formed in the semiconductor substrate and opposed to each other with the gate electrode being interposed between them;

a third impurity diffusion layer formed in a portion immediately below the gate electrode in the semiconductor substrate; and

a sidewall dielectric layer formed on a side surface section of the gate electrode,

wherein the gate electrode has a width that gradually increases from a bottom thereof toward an upper surface thereof, and

wherein surfaces of the first and second impurity diffusion layers are located at a position higher than an interface between the semiconductor substrate and the gate dielectric layer.

21. (Amended) A semiconductor device comprising:

a semiconductor substrate having an indented section;

a gate dielectric layer formed on the indented section;

a gate electrode formed on the gate dielectric layer, wherein a portion of the gate electrode is embedded in the semiconductor substrate and another portion of the gate electrode is above the semiconductor substrate;

first and second impurity diffusion layers formed in the semiconductor substrate and opposed to each other with the gate electrode being interposed between them; and

a sidewall dielectric layer formed on a side surface section of the gate electrode,

wherein the gate electrode has a width that gradually increases from a bottom thereof toward an upper surface thereof,

wherein surfaces of the first and second impurity diffusion layers are located at a position higher than an interface between the semiconductor substrate and the gate dielectric layer, and

wherein surfaces of the first and second impurity diffusion layers are formed at a position higher than a surface of the element isolation region.

28. (Amended) A semiconductor device according to claim 21, further comprising:

a third impurity diffusion layer immediately below the gate electrode in the semiconductor substrate, wherein the third impurity diffusion layer is of the opposite conductivity type as the semiconductor substrate, and wherein the first and second impurity diffusion layers include an extension region.

32. (Amended) A semiconductor device comprising:

a semiconductor substrate having an indented section;

a gate dielectric layer formed on the indented section;

a groove section formed at a specified location in the semiconductor substrate;

a gate electrode formed on the gate substrate and another portion of the gate electrode is above the semiconductor substrate,

wherein the gate electrode has a width that gradually increases from a bottom thereof toward an upper surface thereof, and a width of the upper surface of the gate electrode substantially equals the width of the groove.

Please add the following new claims 33-43:

33. (New) A semiconductor device according to claim 1, wherein the gate electrode is partially interposed between the first and second impurity diffusion layers.

34. (New) A semiconductor device according to claim 1, wherein at least another portion of the gate electrode is above the semiconductor substrate, and the first and second impurity diffusion layers.

35. (New) A semiconductor device according to claim 1, wherein the third impurity diffusion layer is completely disposed between the first and second impurity diffusion layers.

36. (New) A semiconductor device according to claim 1, wherein the extension regions of the first and second impurity diffusion layers are below the sidewall dielectric layer, and wherein an area below the gate dielectric layer is free of the extension regions.

37. (New) A semiconductor device according to claim 21, wherein the gate electrode is partially interposed between the first and second impurity diffusion layers.

38. (New) A semiconductor device according to claim 21, wherein at least another portion of the gate electrode is above the semiconductor substrate, and the first and second impurity diffusion layers.

39. (New) A semiconductor device according to claim 28, wherein the third impurity diffusion layer is completely disposed between the first and second impurity diffusion layers.

40. (New) A semiconductor device according to claim 28, wherein the extension regions of the first and second impurity diffusion layers are below the sidewall dielectric layer, and wherein an area below the gate dielectric layer is free of the extension regions.

41. (New) A semiconductor device according to claim 32, wherein the gate electrode is partially interposed between the first and second impurity diffusion layers.

42. (New) A semiconductor device according to claim 32, wherein a third impurity diffusion layer is completely disposed between the first and second impurity diffusion layers.

43. (New) A semiconductor device according to claim 32, further comprising:

extension regions in the first and second impurity diffusion layers, wherein the extension regions are below the sidewall dielectric layer, and wherein an area below the gate dielectric layer is free of the extension regions.